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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/625,101	07/24/2000	DARRYL BLACK	102689-34	6506

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NUTTER MCCLENNEN & FISH LLP
WORLD TRADE CENTER WEST
155 SEAPORT BOULEVARD
BOSTON, MA 02210-2604

EXAMINER

SHAAWAT, MUSSA

ART UNIT PAPER NUMBER

2128

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/625,101

Applicant(s)

BLACK ET AL.

Examiner

Mussa A Shaawat

Art Unit

2128

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 July 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 November 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 14 December 2000.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to application number 09/625,101. Claims 1-20 are presented for examination.

Claim Objections

2. Claim 12 is objected to because of the following informalities: a dependent claim must claim priority to a precedent claim not to itself. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Kidder et al US Patent No. (6,715,097) referred to hereinafter as Kidder.

4. As to claim 1, Kidder teaches a logical model of a network device, comprising: a first model representing network device hardware (see Fig. 2A block 284 is a hardware model which corresponds to a hardware device); and a second model coupled to the first model and representing network data objects used by processes executable within the network device (see col.8 lines 24-43, comprises objects or devices connected to the hardware model which corresponds to a second model coupled to the first model).

5. As to claim 2, Kidder teaches a logical model of a network device, wherein the first and second models are coupled together through a service endpoint model (see col.8 line 55) and

wherein the first model includes a physical service endpoint (see col.8 line 57) model coupled to the service endpoint model and the second model includes a logical service endpoint (see col.8 line 58) model coupled to the service endpoint model (see col.8 lines 55-58, service endpoint model which includes a physical endpoint model and a logical service endpoint model that couples the first and second model).

6. As to claim 3, Kidder teaches a logical model of claim 1, wherein the first model is capable of representing containment and composes: a plurality of structural models; and a plurality of functional printed circuit board models coupled to the plurality of structural models (see col.8 lines 26-42, shows that the model is capable of showing containment and it composes many structural models).

7. As to claim 4, Kidder teaches a logical model of claim 3, wherein the plurality of structure models comprises a slot model and the plurality of functional printed circuit board models comprises a board model coupled to the slot model (see Fig 2 block 292 shows a slot model, and block 294 shows a printed circuit board models connected together).

8. As to claim 5, Kidder teaches a logical model of claim 3, wherein the plurality of structural models comprises: a chassis model (see Fig 2 block 288); a shelf model coupled to the chassis model (see Fig 2 block 288 shows a chassis model, block 290 shows a shelf model coupled together); and a plurality of functional shelf models coupled to the shelf model (see Fig 2 block 296a...296n, 298 and 300 shows plurality of functional shelf models coupled to the shelf model block 290).

9. As to claim 6, Kidder teaches a logical model of claim 3, wherein the plurality of functional printed circuit board models comprises; a general board model (see Fig. 2 block 294);

and a plurality of functional board models coupled to the general board model (see Fig 2 block 302a...302n, shows plurality of functional board models coupled to a general board model).

10. As to claim 7, Kidder teaches a logical model of claim 3, wherein the plurality of functional board models comprises: a universal port card model (see col.52 line 44); a forwarding card model (see col.52 line 45); a cross-connection card model (see col.52 line 36); and a switch fabric card model (see col.50 line 38).

11. As to claim 8, Kidder teaches a logical mode of claim 7, wherein the first model further comprises: a general port model coupled to the universal port card model (col.51 lines 55-56, shows a physical port table connected to a universal port model); and a physical layer protocol port model coupled to the general port model (see col.8 lines 37-42).

12. As to claim 9, Kidder teaches a logical model of claim 8, wherein the physical layer protocol port model comprises a SONET port model (see col.8 line 41-42).

13. As to claim 10, Kidder teaches a logical model of claim 1, wherein the second model comprises: a plurality of physical layer protocol data object models (see col.9 lines 16-30).

14. As to claim 11, Kidder teaches a logical model of claim 10, wherein the plurality of physical layer protocol data object models comprise: a plurality of SONET data object models (see col.13 lines 7-13).

15. As to claim 12, Kidder teaches a logical model of claim 12, wherein the plurality of physical layer protocol process data objects comprise: a plurality of Ethernet data object models (see col.8 lines 1-5).

16. As to claim 13, Kidder teaches a logical model of claim 1, wherein the second model comprises: a plurality of upper layer protocol data object models (see col.34 lines 53-55).

17. As to claim 14, Kidder teaches a logical model of claim 13, wherein the plurality of upper layer protocol data object models comprise: a plurality of ATM data object models (col.34 lines 65-67).

18. As to claim 15, Kidder teaches a logical model of claim 14, wherein the plurality of upper layer protocol data object models comprise: a plurality of MPLS data object models (col.9 lines 47-48).

19. As to claim 16, Kidder teaches a logical model of claim 14, wherein the plurality of upper layer protocol data object models comprise; a plurality of IP data object models (col.9 lines 47-49).

20. As to claim 17, Kidder teaches a logical model of claim 1, wherein the second model comprises: a plurality of network data objects representing a collection of permanent virtual circuits (see col.9 line 8).

21. As to claim 18, Kidder teaches a logical model of claim 1, wherein the second model comprises: a plurality of network data objects representing a collection of ATM virtual interfaces (see col.9 line 9).

22. As to claim 19, the limitations of claim 19 are similar to the limitations of claim 1; therefore it is rejected based on the same rationale, *supra*.

23. As to claim 20, Kidder teaches a logical model of a network, comprising:
a first model of a first network device comprising (see Fig. 2A block 284 is a hardware model which corresponds to a hardware device): a second model representing the first network device hardware (see col.8 lines 24-43, comprises objects or devices connected to the hardware model which corresponds to a second model coupled to the first model); and a third model coupled to

the second model and representing network data objects used by processes executable within the first network device (see col.8 lines 55-58, service endpoint model which includes a physical endpoint model and a logical service endpoint model that couples the first and second model); and a fourth model of a second network device coupled with the first model of the first network device comprising (see col.8 lines 26-42, shows that the model is capable of showing containment and it composes many structural models): a fifth model representing the second network device hardware (see Fig 2 block 288 shows a block 290 shows a shelf model); and a sixth model coupled to the fifth model and representing network data objects used by processes executable within the second network device (see Fig 2 block 296a...296n, 298 and 300 shows plurality of functional shelf models coupled to the shelf model block 290).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Gardiner et al. US patent No. (5,740,357) generic fault management of a computer system.
- Shimamura US Patent no. (5,682,530) Hierarchical resource management method.
- Barth et al. (5,504,670) method and apparatus for allocating resources in a multiprocessor system.

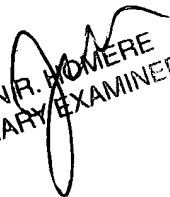
Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mussa A Shaawat whose telephone number is (703) 605-1372. The examiner can normally be reached on Monday-Friday (8:30am to 5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R Homere can be reached on (703) 308-6647. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mussa Shaawat
Examiner
September 28, 2004


JEAN R. HOMERE
PRIMARY EXAMINER